UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,839	10/22/2001	Toshio Yamada	HITA.0112	8390

38327 7590 09/09/2004

REED SMITH LLP
3110 FAIRVIEW PARK DRIVE, SUITE 1400
FALLS CHURCH, VA 22042

EXAMINER	
MENZ, DOUGLAS M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,839	YAMADA ET AL.	
	Examiner	Art Unit	
	Douglas M Menz	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *5, 8-12, 15, 16, 18, 19, 23-29, 32, 38 and 40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7,13,14,17,20-22,30,31,33-37 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, species I, claims 1-4, 6, 7, 13, 14, 17, 20-22, 30, 31, 33-37 and 39, in the reply filed on 5/4/04 is acknowledged.

Drawings

Figure 20 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6, 7, 13, 14, 17, 20-22, 30, 31, 33-37 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujii et al. (US 6274895).

Regarding claim 1, Fujii discloses a semiconductor device comprising a plurality of signal terminals of a circuit block, wherein the signal terminals are arranged along a direction that intersects an extending direction of a wiring which is a wiring of an upper layer and outside the circuit block connected to the signal terminals, and wherein each of the signal terminals is arranged in the direction that intersects the extending direction outside the circuit block so that spaces for a plurality of wiring channels can be secured (Figs. 1-10 and Col. 1, lines: 43-60).

Regarding claim 2, Fujii further discloses wherein a plurality of the circuit blocks are arranged along the extending direction of the wiring outside the circuit blocks and the signal terminals of each of the circuit blocks and the wiring outside the circuit blocks are electrically connected to each other (Figs. 1-10 and Col. 4, lines: 10-45).

Regarding claim 3, Fujii further discloses wherein a wiring area is provided between a group of different circuit blocks among the circuit blocks (Figs. 1-10 and Col. 3, lines: 25-65).

Regarding claim 4, Fujii further discloses wherein the signal terminal is extended in the direction that intersects the extending direction of the wiring outside the circuit block (Col. 7, lines: 1-50).

Regarding claim 6, Fujii further discloses wherein the signal terminal is arranged in a frame of the circuit block (Figs. 1-10).

Regarding claim 7, Fujii further discloses wherein the signal terminal is constituted of a top wiring layer in the circuit block (Figs. 1-10 and Col. 6).

Regarding claim 13, Fujii discloses a semiconductor device comprising:

A plurality of circuit blocks arranged along a first direction (Fig. 1); and

A first wiring that extends to the first direction and electrically connects between the plurality of circuit blocks, wherein a plurality of signal terminals are arranged in each of the plurality of circuit blocks along a second direction that intersects the first direction (Col. 1, lines: 43-60);

Wherein each of the plurality of signal terminals secures spaces for a plurality of wiring channels in the second direction (Figs. 2-10); and

Wherein the first wiring arranged on the wiring layer of the upper layer is electrically connected to each of the plurality of signal terminals (Figs. 2-10 and Col. 4).

Regarding claim 14, Fujii further discloses wherein each of the plurality of signal terminals is extended to the second direction (Figs. 1-10).

Regarding claim 17, Fujii further discloses wherein each of the plurality of signal terminals is constituted of the top wiring layer in the circuit block (Figs. 1-10 and Col. 6).

Regarding claim 20, Fujii further discloses wherein the circuit block is a memory circuit, the first wiring constructs a wiring for an address signal , and the first wiring is connected in common to the circuit block (Figs. 1-10 and Col. 2 – Col. 4).

Regarding claim 21, Fujii further discloses wherein the circuit block is a memory circuit, the first wiring is wiring for data input, and the first wiring is connected in common to the circuit block (Figs. 1-10 and Col. 2 – Col. 4).

Regarding claim 22, Fujii further discloses wherein the circuit block is connected to wiring for a different clock signal (Col. 3, line 25 – Col. 4, line 30).

Regarding claim 30, Fujii further discloses wherein the circuit block is a memory circuit (Col. 2), and

Wherein the signal terminal is formed on the input/output circuit area of the memory circuit (Figs. 1-10).

Regarding claim 31, Fujii further discloses wherein the first wiring is a wiring for an address signal or a wiring for data (Figs. 1-10 and Col. 2 – Col. 4).

Regarding claim 33, Fujii discloses a semiconductor device comprising:

A plurality of memory circuits arranged along a first direction (Fig. 1); and

A plurality of first wiring that are electrically connected to the plurality of memory circuits (Figs. 2-10),

Wherein a signal terminal is arranged in each of the plurality of memory circuits (Figs. 1-10 and Col. 2 – Col. 4) ;

Wherein the plurality of first wiring are formed on the wiring layer of the upper layer of the signal terminal, and extend over the terminal for the signal along the first direction (Figs. 1-10 and Col. 1, lines: 43-60 and Col. 2 – Col. 4);

Wherein each of the signal terminals secures spaces for a plurality of wiring channels in a second direction that intersects the first direction (Figs. 1-10 and Col. 1, lines: 43-60 and Col. 2 – Col. 4); and

Wherein each of the plurality of first wiring is arranged on a different wiring channel in the plurality of wiring channels and is electrically connected to the terminal for the different signal in the signal terminals of the plurality of memory circuits arranged in the first direction (Figs. 1-10 and Col. 1, lines: 43-60 and Col. 2 – Col. 4).

Regarding claim 34, Fujii further discloses further comprising:

A second wiring formed on the same layer wiring layer as the first wiring ,

Wherein the second wiring is electrically connected to each of the signal terminals of the plurality of memory circuits positioned on the same wiring channel (Col. 2 – Col. 4).

Regarding claim 35, Fujii further discloses wherein the first wiring is a wiring for an address signal (Col. 2 – Col. 4).

.

Regarding claim 36, Fujii further discloses wherein the first wiring is a wiring for data (Col. 2 – Col. 4).

.

Regarding claim 37, Fujii further discloses wherein the first wiring is wiring for a clock signal (Col. 2 – Col. 4).

.

Regarding claim 39, Fujii further discloses wherein the first wiring is one of wirings for the address signal and for the data; and

Wherein the second wiring is the other of wirings for the address signal and for the data (Col. 2 – Col. 4).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas M Menz whose telephone number is 571-272-1877. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DM

Christian Wilson
Patent Examiner
AU 2824